

What is claimed is:

1. A method for manufacturing a semiconductor device comprising a data holding portion and a peripheral circuit portion that operates in association with said data holding portion, said data holding portion and said peripheral circuit portion being provided on a same semiconductor substrate, said method comprising the steps of:
 - (a) forming gate interconnections respectively in said data holding portion and said peripheral circuit portion on said semiconductor substrate, each said gate interconnection having its top covered by a silicon nitride film;
 - 10 (b) forming first impurity regions respectively in said data holding portion and said peripheral circuit portion, said respective first impurity regions being formed in the surface of said semiconductor substrate that extend outward from sides of said respective gate interconnections;
 - (c) forming first sidewall nitride films respectively on sides of said gate interconnections in said data holding portion and said peripheral circuit portion;
 - 15 (d) forming second impurity regions respectively in said data holding portion and said peripheral circuit portion, said respective second impurity regions being formed in the surface of said semiconductor substrate that extend outward from sides of said respective first sidewall nitride films;
 - 20 (e) forming a first interlayer insulating film covering said data holding portion and said peripheral circuit portion;
 - (f) selectively removing said first interlayer insulating film on said data holding portion to form first openings that reach the surface of said semiconductor substrate where said first and second impurity regions are formed, and burying a conductive silicon in said first openings to form contact plugs;

(g) after formation of said contact plugs, covering said data holding portion with a resist mask and removing said first interlayer insulating film on said peripheral circuit portion by a wet-etching; and

5 (h) after said step (g), in said peripheral circuit portion, performing a third impurity implantation into the surface of said semiconductor substrate in said peripheral circuit portion using, as an implant mask, said gate interconnection at least having said first sidewall nitride films, so as to form third impurity regions having a higher impurity concentration than said first and second impurity regions.

10 2. The semiconductor device manufacturing method according to claim 1, further comprising the step (i) of, after said step (g) and prior to said step (h), forming an insulating film all over said data holding portion and said peripheral circuit portion and then removing said insulating film in, at least, said peripheral circuit portion by an anisotropic etching, so as to form sidewall insulating films on the sides of said first 15 sidewall nitride films of said gate interconnection,

wherein said step (h) comprises performing said third impurity implantation using, as an implant mask, said gate interconnection in said peripheral circuit portion on which said sidewall insulating films are formed.

20 3. The semiconductor device manufacturing method according to claim 1, further comprising, after said step (h), the step (j) of forming a metal silicide film on the surface of said semiconductor substrate in, at least, said peripheral circuit portion where said third impurity regions are formed.

25 4. The semiconductor device manufacturing method according to claim 2,

wherein said step (i) comprises removing said insulating film in said peripheral circuit portion, with said insulating film on said data holding portion protected from said anisotropic etching, and

5 said semiconductor device manufacturing method further comprises, after said step (h), the step (j) of forming a metal silicide film on the surface of said semiconductor substrate in said peripheral circuit portion where said third impurity regions are formed.

10 5. The semiconductor device manufacturing method according to claim 2,
 wherein said step (i) comprises removing said insulating film also on said data holding portion by said anisotropic etching, and

15 said semiconductor device manufacturing method further comprises, after said step (h), the step (j) of forming metal silicide films respectively on all said contact plugs in said data holding portion and on the surface of said semiconductor substrate in said peripheral circuit portion where said third impurity regions are formed.

15 6. The semiconductor device manufacturing method according to claim 4,
 wherein said step (i) comprises forming said insulating film with a silicon oxide film, and

20 said semiconductor device manufacturing method further comprises, after said step (j), the steps of:

 removing said silicon oxide film by a wet-etching and forming a second interlayer insulating film covering said data holding portion and said peripheral circuit portion; and

25 forming, in a self-aligned manner, contact openings passing through said second interlayer insulating film on said data holding portion and said peripheral circuit

portion to respectively reach said contact plugs and said metal silicide film.

7. The semiconductor device manufacturing method according to claim 5,
wherein said step (i) comprises forming said insulating film with a silicon oxide
5 film, and

said semiconductor device manufacturing method further comprises, after said
step (j), the steps of:

removing said silicon oxide film by a wet-etching and forming a second
interlayer insulating film covering said data holding portion and said peripheral circuit
10 portion; and

forming, in a self-aligned manner, contact openings passing through said
second interlayer insulating film on said data holding portion and said peripheral circuit
portion to respectively reach said metal silicide films.

15 8. The semiconductor device manufacturing method according to claim 4,
wherein said step (i) comprises forming said insulating film with a silicon
nitride film, and

said semiconductor device manufacturing method further comprises, after said
step (j), the steps of:

20 forming a second interlayer insulating film covering said data holding portion
and said peripheral circuit portion; and

forming, in a self-aligned manner, contact openings passing through said
second interlayer insulating film on said data holding portion and said peripheral circuit
portion to respectively reach said contact plugs and said metal silicide film.

9. The semiconductor device manufacturing method according to claim 5,
wherein said step (i) comprises forming said insulating film with a silicon
nitride film, and

5 said semiconductor device manufacturing method further comprises, after said
step (j), the steps of:

 forming a second interlayer insulating film covering said data holding portion
and said peripheral circuit portion; and

 forming, in a self-aligned manner, contact openings passing through said
second interlayer insulating film on said data holding portion and said peripheral circuit
portion to respectively reach said metal silicide films.

10. The semiconductor device manufacturing method according to claim 4,
wherein said step (i) comprises forming said insulating film as a two-layered
film in which a silicon oxide film is formed on a silicon nitride film and said sidewall
insulating films are formed of a two-layered film composed of a sidewall nitride film and
15 a sidewall oxide film, and

 said semiconductor device manufacturing method further comprises, after said
step (j), the steps of:

 removing said silicon oxide film by a wet-etching and forming a second
20 interlayer insulating film covering said data holding portion and said peripheral circuit
portion; and

 forming, in a self-aligned manner, contact openings passing through said
second interlayer insulating film on said data holding portion and said peripheral circuit
portion to respectively reach said contact plugs and said metal silicide film.

11. The semiconductor device manufacturing method according to claim 1, wherein said step (f) comprises forming said contact plugs also at a border between said data holding portion and said peripheral circuit portion.

5 12. A semiconductor device comprising a data holding portion and a peripheral circuit portion that operates in association with said data holding portion, said data holding portion and said peripheral circuit portion being formed on a same semiconductor substrate, said semiconductor device comprising:

10 gate interconnections provided respectively in said data holding portion and said peripheral circuit portion on said semiconductor substrate, each said gate interconnection having its top covered by a silicon nitride film;

 first sidewall nitride films provided respectively on sides of said gate interconnections in said data holding portion and said peripheral circuit portion;

15 first and second impurity regions provided in said data holding portion and said peripheral circuit portion, said respective first and second impurity regions being selectively formed in the surface of said semiconductor substrate that extend outward from sides of said respective gate interconnections;

 sidewall insulating films provided on sides of said first sidewall nitride films of said gate interconnection in said peripheral circuit portion;

20 contact plugs composed of a conductive silicon and passing through a first interlayer insulating film provided on said data holding portion to reach the surface of said semiconductor substrate where said first and second impurity regions are formed;

 third impurity regions provided in said peripheral circuit portion, said third impurity regions being selectively formed in the surface of said semiconductor substrate that extend outward from sides of said sidewall insulating films and having a higher

impurity concentration than said first and second impurity regions; and metal silicide films provided on all said contact plugs in said data holding portion and on the surface of said semiconductor substrate in said peripheral circuit portion where said third impurity regions are formed.

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13. The semiconductor device according to claim 12, wherein said sidewall insulating films are second sidewall nitride films.

10 14. The semiconductor device according to claim 12, further comprising:
a second interlayer insulating film provided to cover said peripheral circuit portion and said first interlayer insulating film in said data holding portion; and
bit line contacts formed in a self-aligned manner to pass through said second interlayer insulating film on said peripheral circuit portion and on said first interlayer insulating film in said data holding portion to respectively reach said metal silicide films.

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15. A semiconductor device comprising a data holding portion and a peripheral circuit portion that operates in association with said data holding portion, said data holding portion and said peripheral circuit portion being formed on a same semiconductor substrate, said semiconductor device comprising:

20 gate interconnections provided respectively in said data holding portion and said peripheral circuit portion on said semiconductor substrate, each said gate interconnection having its top covered by a silicon nitride film;

first sidewall nitride films provided respectively on sides of said gate interconnections in said data holding portion and said peripheral circuit portion;

25 first and second impurity regions provided in said data holding portion and said

peripheral circuit portion, said respective first and second impurity regions being selectively formed in the surface of said semiconductor substrate that extend outward from sides of said respective gate interconnections;

5 sidewall insulating films provided on sides of said first sidewall nitride films of said gate interconnection in said peripheral circuit portion;

contact plugs composed of a conductive silicon and passing through a first interlayer insulating film provided on said data holding portion to reach the surface of said semiconductor substrate where said first and second impurity regions are formed;

10 third impurity regions provided in said peripheral circuit portion, said third impurity regions being selectively formed in the surface of said semiconductor substrate that extend outward from sides of said sidewall insulating films and having a higher impurity concentration than said first and second impurity regions; and

a metal silicide film provided only on the surface of said semiconductor substrate in said peripheral circuit portion where said third impurity regions are formed.

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16. The semiconductor device according to claim 15, wherein said sidewall insulating films are second sidewall nitride films.

20 17. The semiconductor device according to claim 15, further comprising:
a second interlayer insulating film provided to cover said data holding portion and said peripheral circuit portion; and

bit line contacts formed in a self-aligned manner to pass through said second interlayer insulating film on said data holding portion and said peripheral circuit portion to respectively reach said contact plugs and said metal silicide film.

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